High Performance, Minimal Power

How OpenHW Foundation's CV32E20X core and CV-X-IF interface helped unlock performance and efficiency gains in AI, image, and signal processing for Synthara

About Synthara

Founded in 2019, leading Swiss semiconductor organisation Synthara AG focuses on in-memory computing (IMC) – an emerging paradigm that tightly integrates computation and memory to improve efficiency and performance.

Synthara works with foundries, chip manufacturers, and industry partners to bring this technology into real-world applications, ranging from personalised wearables to autonomous robots,and smart sensor networks.

When area and power budgets are critical

As a member of the EU-funded TRISTAN project, Synthara aimed to evaluate various options for integrating custom accelerators, or its own IMC technology, into RISC-V CPUs for use in small devices, such as wearables. With demand consistently growing for application-specific optimizations, and AI models evolving faster than hardware can keep pace, Synthara sought a highly customizable, extensible, and scalable solution – choosing to create a co-processor equipped with a custom Instruction Set Architecture (ISA) that included several non-standard RISC-V operations.

Given considerable size constraints, the team chose to leverage the lightweight CV32E20X core alongside the CORE-V eXtension interface X-IF), developed and maintained by the OpenHW Foundation, which communicated with Synthara's co-processor.

"In order to meet the power and area constraints imposed in wearable applications, we leveraged

RISC-V's built-in capability to add application-specific instructions. By exploiting the CV-X-IF, we were able to add these instructions without touching the internal pipeline of the CV32E20X, reducing project and schedule risk." Maurizio Capra, Project Leader for Synthara in Tristan.

Using a co-processor to implement custom ISA extensions enabled Synthara to offload specialized tasks from the main CPU, allowing for parallel processing and freeing the primary core to handle general-purpose workloads. At the same time, the approach boosted overall system performance and helped manage power consumption more effectively.

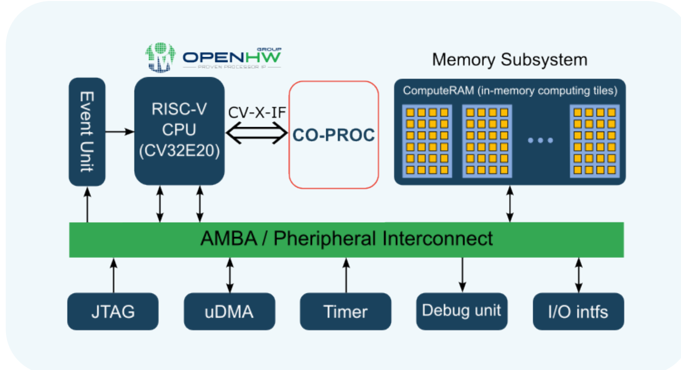
"Extending a CPU by adding more functionalities inside the pipeline is immensely complex. Then, once you dive into the code and customize it for your particular use case, you need to reverify the CPU. That in itself is a lengthy and tough job. Using a co-processor and the CV-X-IF interface was the obvious choice for us," said Capra.

Architecture

At the core of Synthara's solution is the RISC-V CV32E20 CPU, which communicates with a specialized co-processor through the CV-X-IF interface.

The memory subsystem features several tiles of Synthara's ComputeRAM™ – an advanced in-memory computing technology that performs computations directly within the memory array, significantly reducing data transfer bottlenecks and improving efficiency.

The architecture is interconnected via an AMBA/Peripheral Interconnect, facilitating communication between the CPU, co-processor, memory subsystem, and various peripheral units such as the Event Unit, JTAG, uDMA, Timer, Debug Unit, and I/O interfaces. This interconnect ensures efficient data flow and coordination among all components, enabling the system to achieve high performance and low power consumption.



SA extension

The co-processor implements a custom ISA that includes several non-standard operations not ratified by any official RISC-V organization. These operations support different data parallelism modes, such as half-word (16-bit), byte (8-bit), and mixed precision (16-bit and 8-bit). This flexibility allows for optimized processing of various computational tasks, enhancing performance and energy efficiency.

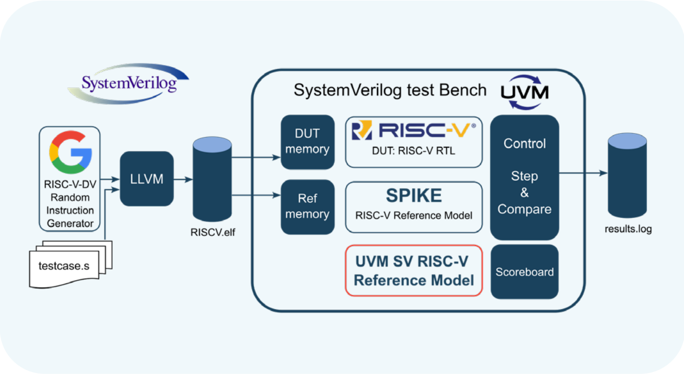
In-memory computing

ComputeRAM™, an advanced in-memory computing tile, enables computations to be performed directly where the data resides, eliminating the need for extensive data movement between the CPU and memory. This integration accelerates processing and enhances energy efficiency, making it ideal for edge AI and IoT applications

Verification

The verification process leveraged SystemVerilog and UVM methodologies. Starting with Chips Alliance RISC-V-DV random instruction generator or specific test cases, source code was compiled using an LLVM toolchain, which accommodates both the ISA extension and the in-memory compute tiling to produce an executable .elf file.

This executable was used to set up the Device Under Test simulation and the instruction set simulator – Spike. The simulation ran in step-and-compare mode to verify the correct functioning of the core.



Outcomes

Synthara's work integrating custom ISA extensions and in-memory computing into a RISC-V-based system architecture significantly enhanced processing speed and energy efficiency – crucial for meeting the demands of modern computational tasks, particularly in edge AI and IoT applications.

"When we designed this co-processor, we aimed for area and power – trying to be smaller and keep power as low as possible. The CV-X-IF certainly contributed to the development and design. It was a huge time saver. Without touching the CPU, we were able to design and verify much faster simply by developing a tiny co-processor, as we only needed to verify the co-processor itself.

"Because the OpenHW Foundation defined this standard, it is reusable and interoperable with other RISC-V cores that support the standard. This is ideal because you can scale up or down and use different CPUs, but the interface can remain the same," said Capra.

Early benchmarks also indicate that Synthara's ComputeRAM™ could drastically improve performance – making it an ideal component for boosting the capabilities of microcontroller-based systems without extensive modifications to existing memory architectures. When used in place of SRAM, it unlocks 100x performance and efficiency gains in AI, image, and signal processing on any microcontroller-based platform across a wide range of applications, including wearables, IoT, and smart sensing.

What's next?

Synthara plans to extend its work by building hybrid platforms capable of supporting multiple CPU architectures while continuing to rely on co-processor modularity for workload acceleration. The company's long-term vision is to integrate custom ISAs for customer-specific needs while maintaining flexibility, low power, and scalability in edge devices.

Synthara is also contributing its innovations back into the RISC-V ecosystem – the CV32E20X core, co-processor, and the verification environment will be released open source, under the stewardship of the OpenHW Foundation, as part of the TRISTAN project.